

## CLAIMS

What is claimed is:

1           1. A monolithic array amplifier comprising:  
2           a plurality of amplification units arranged in a grid-like structure on a  
3           monolithic substrate; and  
4           a grid-bias network separating the amplification units to provide DC power  
5           to the amplification units,  
6           wherein each amplification unit comprises bias-line bypass circuits in a  
7           periodic structure.

1           2. The array amplifier of claim 1 wherein each bias-line bypass circuit is  
2           positioned along bias streets of the grid-bias network and the bias-line bypass  
3           circuits are positioned at least partially around each amplification unit within a  
4           grid unit to reduce RF current flow between an associated one of the amplification  
5           units and the grid-bias network.

1           3. The array amplifier of claim 1 wherein each bias-line bypass circuit  
2           includes resistive-inductive-capacitance networks comprising:  
3           thin-film capacitors;  
4           inductive wire bridges coupling the capacitors to bias streets of the grid-  
5           bias network; and  
6           thin-film resistors coupling the capacitors to ground vias.

1           4. The array amplifier of claim 3 wherein the capacitors of each bias line  
2           circuit have differing values selected to resonate with the inductive wire bridges  
3           and the thin-film resistors to shunt RF current flow over a range of RF  
4           frequencies.

1           5. The array amplifier of claim 3 further comprising second thin-film  
2           capacitors coupled between more than one ground vias with second thin-film

3 resistors, and further coupled with the grid-bias network with second inductive  
4 wire bridges.

1 6. The array amplifier of claim 3 wherein the inductive wire bridges  
2 comprise inductive wire-bridge fuses, the fuses to provide an open circuit when an  
3 associated one the thin-film capacitors shorts to ground.

1 7. The array amplifier of claim 1 wherein the monolithic substrate  
2 comprises a semiconductor material, and wherein the bias-line bypass circuits are  
3 positioned along a bias street of the grid-bias network and spaced apart by less  
4 than a quarter-wavelength of an effective propagation constant of the bias street,  
5 and  
6 wherein the semiconductor material comprises a material selected from the  
7 group consisting of Indium-Phosphide (InP), Gallium Arsenide (GaAs), Gallium  
8 Nitride (GaN), and Silicon (Si).

1 8. The array amplifier of claim 1 wherein each amplification unit  
2 comprises a power amplifier which receives a bias voltage from the grid-bias  
3 network.

1 9. The array amplifier of claim 7 wherein the power amplifier comprises a  
2 self-biased high-electron-mobility transistor (HEMT) amplifier.

1 10. The array amplifier of claim 1 wherein at least some of the  
2 amplification units of the plurality comprise:  
3 a receive antenna;  
4 a transmit antenna; and  
5 a power amplifier to receive a bias voltage from the grid-bias network and  
6 to amplify millimeter-wave frequencies received by the receive antenna for  
7 transmission by the transmit antenna.

1 11. The array amplifier of claim 10 wherein the receive antennas are  
2 configured to receive a substantially vertically-polarized wavefront at a

3 millimeter-wave frequency, the power amplifiers are configured to amplify signals  
4 to provide a substantially horizontally-polarized wavefront, and the transmit  
5 antennas are configured to transmit the amplified signals to generate the high-  
6 power collimated wavefront at the millimeter-wave frequency.

1 12. The array amplifier of claim 3 wherein the grid-bias network comprises  
2 a mesh structure comprising gold having a thickness of approximately between 20  
3 and 30 microns and a width between approximately 200 and 400 microns,  
4 wherein a power source provides up to 300 amps of current to the grid-bias  
5 network, and wherein the capacitors range between approximately 0.05pf and  
6 10.0pf.

1 13. A method of decoupling a bias structure in a monolithic array amplifier  
2 comprising:  
3 providing DC power to a plurality of amplification units arranged in a  
4 grid-like structure with a grid-bias network separating the amplification units; and  
5 reducing RF current flow between the amplification units and the grid-bias  
6 network with a periodic structure of bias-line bypass circuits within each of the  
7 amplification units.

1 14. The method of claim 13 wherein reducing comprises shunting RF  
2 current flow over a range of RF frequencies with a plurality of RLC networks that  
3 comprise each bias-line bypass circuit, each bias-line bypass circuit comprising  
4 thin-film capacitors, inductive wire bridges coupling the capacitors to bias streets  
5 of the grid-bias network, and thin-film resistors coupling the capacitors to ground  
6 vias, wherein the capacitors of each bias line circuit have differing values selected  
7 to resonate with an associated one of the thin-film resistors and an associated one  
8 of the inductive wire bridges.

1 15. The method of claim 14 further comprising:  
2 providing second thin-film capacitors between more than one of the  
3 ground vias, the second thin-film capacitors coupled to the more than one of the  
4 ground vias with second thin-film resistors; and

5 providing second inductive wire bridges coupling the second thin-film  
6 capacitors with the grid-bias network.

1 16. The method of claim 14 wherein the inductive wire bridges comprise  
2 inductive wire-bridge fuses, and the method further comprises providing an open  
3 circuit with the inductive wire-bridge fuses when an associated one the thin-film  
4 capacitors shorts to ground.

1 17. The method of claim 13 wherein the monolithic substrate comprises a  
2 semiconductor material, and wherein reducing comprises positioning the bias-line  
3 bypass circuits along a bias street of the grid-bias network to have a spacing of  
4 less than a quarter-wavelength of an effective propagation constant of the bias  
5 street.

1 18. The method of claim 13 wherein at least some amplification units of  
2 the plurality comprise a receive antenna, a transmit antenna, and a power  
3 amplifier.

1 19. The method of claim 18 further comprising:  
2 providing each power amplifier with a bias voltage from the grid-bias  
3 network; and  
4 amplifying millimeter wave signals received by the receive antenna for  
5 transmission by the transmit antenna.

1 20. A bias-line bypassing structure comprising a plurality of bias-line  
2 bypass circuits positioned in a periodic structure at least partially around each of a  
3 plurality of circuit elements to reduce RF current flow between the circuit  
4 elements and a grid-bias network for providing bias current to the circuit elements.

1 21. The structure of claim 20 wherein each bias-line bypass circuit  
2 comprises thin-film capacitors, inductive wire bridges coupling the capacitors to  
3 bias streets of the grid-bias network, and thin-film resistors coupling the  
4 capacitors to ground vias, wherein the capacitors have differing values selected to

5 resonate with an associated one of the inductive wire bridges and an associated  
6 one of the thin-film resistors to shunt RF current flow over a range of RF  
7 frequencies.

1           22. The structure of claim 21 wherein the inductive wire bridges comprise  
2 inductive wire-bridge fuses, the fuses to provide an open circuit when an  
3 associated one the thin-film capacitors shorts to ground.

1           23. The structure of claim 21 wherein the plurality of circuit elements are  
2 arranged in a grid-like structure and fabricated on a single monolithic substrate,  
3 the plurality of circuit elements and the bias-line bypass circuits being within grid  
4 units separated by bias streets which form the structure.

1           24. The structure of claim 22 wherein the grid-bias network is power-grid  
2 mesh separating the circuit elements for providing DC power to the circuit  
3 elements.

1           25. The structure of claim 20 wherein the bias-line bypass circuits further  
2 comprise second thin-film capacitors coupled between more than one ground vias  
3 with second thin-film resistors, and coupled with the grid-bias network with  
4 second inductive wire bridges.

1           26. The structure of claim 23 wherein the monolithic substrate comprises a  
2 semiconductor material, and wherein the bias-line bypass circuits are positioned  
3 along the bias streets of the grid-bias network and spaced apart by less than a  
4 quarter-wavelength of an effective propagation constant of the bias street.

1           27. The structure of claim 26 wherein the semiconductor material  
2 comprises a material selected from the group consisting of Indium-Phosphide  
3 (InP), Gallium Arsenide (GaAs), Gallium Nitride (GaN), and Silicon (Si).

1           27. The structure of claim 21 wherein each circuit element comprises a  
2 receive antenna, a transmit antenna, and a power amplifier to receive a bias

3 voltage from the grid-bias network and to amplify a millimeter wave signals  
4 received by the receive antenna for re-transmission by the transmit antenna.

1 28. The structure of claim 21 wherein the grid-bias network comprises a  
2 mesh structure comprised of gold having a thickness of approximately between 20  
3 and 30 microns and a width between approximately 200 and 400 microns.

1 29. The structure of claim 28 wherein a power source provides up to 300  
2 amps of current to the grid-bias network, and wherein the capacitors range  
3 between approximately 0.05pf and 10.0pf.